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A comprehensive study and analysis of second order harmonic ripple in DC microgrid feeding single phase PWM inverter loads

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***Abstract*—The paper presents a detailed analysis of second order harmonic ripple in a DC microgrid. A boost converter feeding PWM inverter load is considered and equivalent circuit is proposed. The effect of the size of input capacitor, output capacitor and inductor of boost converter, on this ripple has been investigated. The proposed model has been validated through experimentation and simulation.**

I. INTRODUCTION

DC distributed generation units (DGUs) like solar PVs, wind turbine, fuel cells etc, storage like battery, ultra capacitors etc and low/medium voltage loads together constitute a power system entity known as DC microgrid. The power converters are indispensable parts while connecting DGUs and storage to dc bus in DC microgrid. However, loads can be connected directly or through power conversion stage. AC load requires an inverter to interface with DC microgrid. Furthermore, the AC loads supplied by DGUs, are generally connected at DC bus through the front end single phase pulse width modulated inverters (SPPWMIs) for low/medium power application. In such systems, a second order harmonic current (SHC) ripple or voltage pulsation is generally noticed at DC terminals. For instance, if an AC load is supplied with $50/60$ Hz frequency using $1-\phi$ inverter, then a ripple with $100/120Hz$ frequency appears at DC input terminal. Moreover, if the compensation of this ripple is ignored at DC connection points, then the ripple can propagate towards the input dc sources also. Continuous propagation of the ripple through components of the power converters may result into damage or instabilities in the DC microgrid. Some of the problems introduced by SHC in a DC microgrid are: (a) Large perturbation of DC link voltage [1]; European standard $(EN50160)$ suggests that the maximum values of second order low frequency ripple in nominal mean voltage at the DC supply end must be limited within 2% of it, (b) Nuisance tripping of maximum power point tracker (MPPT) [2]; for achieving a utilization factor of 98%, the amplitude of ripple in MPPT voltage must be less than 8.5% [3], (c) Hysteresis effect in fuel cells and battery causes heating; for the $Nexa$, $1.2\ kW$ fuel cell, current ripple at $120\ Hz$ should be limited to 24.7% root mean square (RMS) value of fuel cell current [4], and according to [2], ripple in current greater than 8% of its DC value, may cause excessive stress and loss in the fuel cell, (d) Light flickering may causes eyes health problem [5], and (e) Increase in AC load connected through inverter, increases insulation and component stress, and distortion in the inverter output waveform [6]. Two most common methods to minimize the ripple component are passive and active compensation method. Under the passive compensation, a large size DC link electrolytic capacitor is generally used at DC bus to bypass and absorb ripple component. However, low ripple handling capability and high equivalent series resistance (ESR) of electrolytic capacitor, shorten its life $(1000-7000$ hrs at 105^0C [5]). An alternative of electrolytic capacitor is film capacitor [7]. ESR of film capacitor is low while the ripple current handing capacity is very high in comparison to electrolytic capacitor. This results in increased life span of thin film capacitor [5]. Drawbacks associated with passive compensation technique motivate active ripple compensation methods. There are many active compensation techniques which can be further classified broadly in two categories: (a) Power converter self controlling ripple compensation method [1]; this method do not add any auxiliary circuit to main circuit (b) Ripple current injection method; this adds extra auxiliary circuit to main system [8], [9].

This paper presents detailed analysis of SHC ripple using boost converter. An equivalent circuit of boost converter has been developed and the effect of different elements of boost converter, on the SHC has been analyzed. The equivalent circuit has been validated experimentally. The paper follows with introduction of a typical DC microgrid feeding SPPWMI loads in the Section II. Modeling and equivalent circuit development of boost converter has been covered in the Section III. In the Section IV, ripple currents calculation has been done. SHC analysis has been covered in the Section V. System validation is done in section VI. Finally, Section VII concludes the paper.

II. A TYPICAL DC MICROGRID FEEDING AC LOADS WITH THE FRONT END SINGLE PHASE PWM INVERTER

A typical DC microgrid feeding DC and AC composite loads is shown in Fig.1. DC micro (μ)-sources are connected to DC source bus through MPPT and voltage regulator (boost converter). Source bus voltage has been stepped down using buck converter, and fed to a DC load bus. DC load bus feeds low voltage DC and AC loads. Energy storage systems

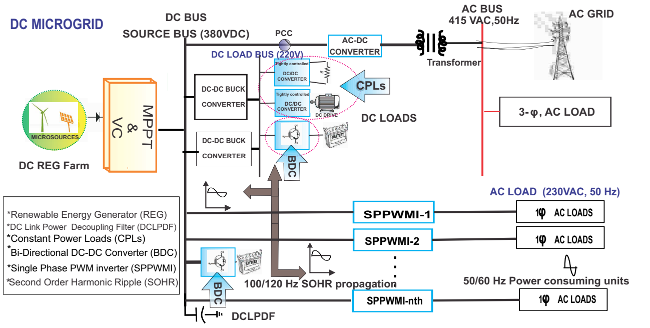

Fig. 1. A typical DC microgrid feeding AC loads with front end SPPWMIs

are connected to each dc bus through bidirectional DC-DC converters. The DC microgrid can also be connected to main grid for grid connected operation as shown in Fig.1. AC loads are connected to source bus through front end PWM inverter. SHC ripple is also shown in this figure. SHC ripple in the input current of inverter, $(i_{2\omega})$, and the capacitance, (C) required at dc link, to compensate this SHC are given by [10],

$$i_{2\omega} = \frac{Pcos(2\omega t)}{V_o} \quad and \quad C = \frac{P}{4\omega \Delta V_{p-p} V_o} \tag{1}$$

Here, V_o and ΔV_{p-p} are input average DC voltage of inverter and peak to peak SHC ripple in it. P_{rms} and ω are AC load RMS power and frequency. In the next section, modeling of boost converter feeding AC load with front end SPPWMI is covered.

III. Boost Converter With Inverter Load

A. Modeling of Boost Converter Feeding Single Phase Inverter Loads

A circuit of non-ideal boost converter feeding AC load with front end SPPWMI is shown in Fig.2. The inverter is modeled as a current source. In Fig.2, x_1, x_3, x_L are inductor current, input current and load current, x_2 and E are output capacitor voltage and input voltage, D is duty cycle $(D' = (1-D))$. L is inductance, and C_1 and C_2 are input and output capacitance. r_S and r_D are ON-time resistance of switch and diode respectively. V_D is On-time voltage drop of diode. r_E, r_L, r_1 and r_2 are equivalent series resistances (ESRs) of input source, inductor, input and output capacitor.

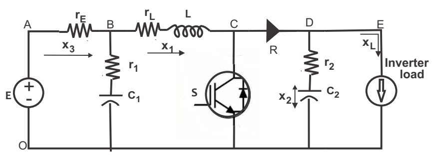

Fig. 2. Non-ideal boost converter feeding single phase inverter load

1) Average Model: The average model of boost converter shown in Fig.2 can be given as follows,

$$\begin{aligned} L\dot{x_1} = E - r_E x_3 - (r_L + r_S D + (r_D + r_2)D')x_1 \\ -V_D D' - x_2 D' + r_2 D' x_L \end{aligned} \tag{2a}$$

$$C_2 \dot{x_2} = D' x_1 - x_L \tag{2b}$$

2) Perturbation: In order to investigate the dynamic behavior of the system with SHC, state variables are perturbed around DC steady state variables. The new state variables can be given as: *Dynamic model state variables=DC steady state components + small signal AC components*

$$\begin{aligned} x_1 := I_L + i_L, x_2 := V_o + v, x_3 := I_E + i_E, \\ x_L := I_o + i_o, D = D_o + d \end{aligned} \tag{3}$$

Here, I_L, V_o, I_E, I_o, D_o and i_L, v, i_E, i_o, d are steady state and ripple component of the variable respectively. EMF of the source is fixed and lets assume source voltage will vary only because of its internal resistance. Using (2) and (3), an average small signal model with inductor current dynamics given by (4) and output voltage dynamic given by (5), is developed. Dynamics of average model are separated in DC steady state terms, first order AC terms and second order AC terms.

$$\begin{aligned} L\dot{I_L} + L\dot{i_L} = [E - r_2 I_E - I_L(r_L + r_S D_o \\ +(r_D + r_2)D_o') - (V_D + V_o + r_2 I_o)D_o] \\ [Steady\ State\ Terms] \\ +[-r_E i_E - (r_L + r_S D_o + (r_D + r_2)D_o')i_L - ((r_S - \\ r_D - r_2)I_L - V_D - V_o + r_2 I_o)d - vD_o'] \\ [1^{st}\ Order\ AC\ Terms] \\ +[-(r_S - (r_D + r_2))di_L + vd - r_2 i_o]d \\ [2^{nd}\ Order\ AC\ Terms] \end{aligned} \tag{4}$$

$$\begin{aligned} C_2\dot{V} + C_2\dot{v} = D_o' I_L - I_o\ [DC\ Terms] \\ +D_o' I_L - dI_L - i_o \quad [1^{st}\ order\ AC\ Terms] \\ -di_L \quad [2^{nd}\ Order\ AC\ Terms] \end{aligned} \tag{5}$$

3) Small Signal AC Model: To obtain a small signal AC model, all steady-state DC terms and 2^{nd} order (cross-product) AC terms are dropped in (4) and (5). Collecting the first order AC terms together gives the following model,

$$\begin{aligned} L\dot{i_L} = -r_E i_E - (r_L + r_S D_o + (r_D + r_2)D_o')i_L \\ -((r_S - r_D - r_2)I_L - V_d - V_o + r_2 I_o)d - vD_o' \end{aligned} \tag{6a}$$

$$C_2 \dot{v} = D_o' i_L - dI_L - i_o \tag{6b}$$

Now, this model is transformed in s-domain using Laplace transform as follows.

$$\begin{aligned} sLi_L(s) = -r_E i_E(s) - (r_L + r_S D_o + (r_D + r_2)D_o') \\ i_L(s) - ((r_S - r_D - r_2)I_L(s) - V_d - V_o \\ +r_2 I_o)d(s) - v(s)D_o' \end{aligned} \tag{7a}$$

$$sC_2 v(s) = D_o' i_L(s) - d(s)I_L - i_o(s) \tag{7b}$$

This model helps in designing of equivalent circuit for the analysis of SHC riiple around the frequency of interest i.e. $\omega_2 = 2\omega$ (100 Hz, in our case).

B. Equivalent Circuit

In this section, using the small signal AC model, an equivalent circuit has been developed. Steps for equivalent circuit development are as follows,

STEP-I Average switching circuits design:- Using Laplace model given by (7), two circuits for each dynamics (i.e. inductor current and output capacitor voltage dynamics) has been designed as shown in the Fig.3a.

STEP-II Transformer equivalent circuit design: Convert combination of dependent voltage and current source into an effective ideal transformer with transformer ratio of $(D'_o : 1)$ as shown in Fig.3b. This has been done by assuming that the DC-DC converter switches at a very high frequency.

STEP-III Equivalent ripple circuit design: Finally, we have a circuit with an ac transformer. To develop equivalent ripple circuit, transfer primary side impedances to secondary side as shown in Fig.3c. The current is multiplied by D'_o and voltage is divide by D'_o. The impedance is divided by ${D'_o}^2$. In the next

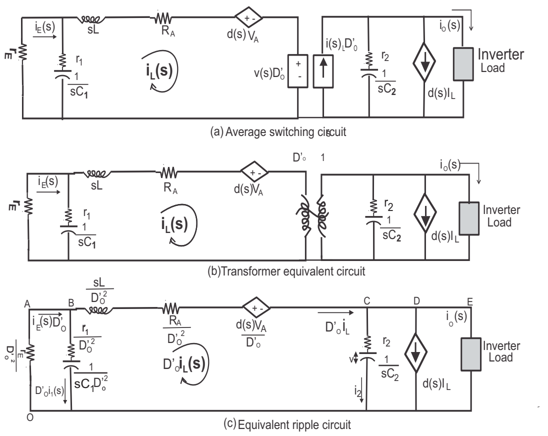

Fig. 3. Equivalent ripple circuit development

section, this equivalent ripple model has been used for SHC analysis.

IV. Branch Impedance And Input Source Current Ripple Calculation

In this section calculation of impedance of each branch of AC equivalent ripple circuit of boost converter has been done. The purpose of this calculation is to calculate the part of output current ripple in each branch of the equivalent circuit of the boost converter, and hence finally calculate the second order harmonic ripple in input source.

A. Impedance of Each Branch of Equivalent Ripple Circuit

The impedance of each branch can be calculated as follows, Using circuit shown in Fig.3c,

$$Impedance\ of\ branch\ 'OAB',\ Z_E = \frac{r_E}{{D'_o}^2} \tag{8a}$$

$$Impedance\ of\ branch\ 'BO',\ Z_1 = \frac{r_1}{{D'_o}^2} + \frac{1}{sC_1{D'_o}^2} \tag{8b}$$

$$Impedance\ of\ branch\ 'BC',\ Z_{Lr} = \frac{sL}{{D'_o}^2} + \frac{R_A}{{D'_o}^2} \tag{8c}$$

$$Impedance\ of\ branch\ 'CO'\ Z_2 = r_2 + \frac{1}{sC_2} \tag{8d}$$

Here, $R_A = r_L + r_S D_o + (r_D + r_2)D'_o$. The combined impedance of branch 'OABO Branch'

$$Z_{E1} = \frac{sC_1 r_E(r_1+1)}{{D'_o}^2[sC_1(r_1+r_E)+1]} \tag{9}$$

B. Current Ripple Propagating to Input Source

Using the branch impedances, branch currents has been calculated in this section. A relation among the output current ripple, duty variation and inductor current ripple has been derived. Finally, an mathematical expression for input source current ripple has been deduced using this relation.

$$i_L(s) = \frac{[C_1C_2(A_1i_o(s)+A_2d(s))]s^2 + [(A_3C_1+A_4C_2)i_o(s)+(A_5C_1+A_6C_2)d(s)]s + A_7d(s) + A_oi_o(s)}{A_8LC_1C_2s^3 + (A_9C_1C_2+LC_2)s^2 + (A_3A_0C_1+A_{10}C_2)s + A_0^2} \tag{10}$$

1) Inductor current ripple (i_L): Applying KCL at Node C in Fig.3c,

$$i_L(s) = \frac{(i_o(s) + dI_L + i_2(s))}{D'_o} \tag{11}$$

Also, applying KVL in OABCO loop,

$$i_2(s) = -(\frac{(Z_{E1}+Z_{Lr})D'_oi_L(s)}{Z_2} + \frac{d(s)V_A}{Z_2D'_o}) \tag{12}$$

Here, $V_A = ((r_S - r_D - r_2)I_L - V_D - V_o + r_2I_o)$. Now, using (11) and (12),

$$i_L(s) = \frac{Z_2D'_o(i_o(s)+d(s)I_L) - d(s)V_A}{{D'_o}^2(Z_2+Z_{E1}+Z_{Lr})} \tag{13}$$

Further solving (13), using (8c), (8d) and (9) gives (10). Lets $\alpha = r_2D'_o, \beta = r_E(r_1+1), \gamma = r_1 + r_E, \delta = r_E - r_1$ and $\mu = r_E + 2r_1$. So, the constants in (10) are $A_o = D'_o, A_1 = \alpha\gamma, A_2 = \gamma A_6, A_3 = \gamma D'_o, A_4 = \alpha; A_5 = \gamma I_L D'_o, A_6 = \alpha I_L - V_A, A_7 = I_L D'_o, A_8 = \gamma, A_9 = (\alpha\gamma D'_o + \gamma R_A + \beta), A_{10} = \alpha D'_o + R_A$, Clearly, the indutcor current ripple, i_L depends on small change in duty, $d(s)$ and output current ripple, $i_o(s)$. This relation can further be used for calculation of input source ripple current.

2) Input source current ripple (i_E): Applying KCL at Node-B in Fig.3c

$$i_E(s) = i_1(s) + i_L(s) \tag{14}$$

Also, applying KVL in OABO loop,

$$i_1(s) = \frac{Z_Ei_E(s)}{Z_1} \tag{15}$$

Using (14) & (15)

$$i_E(s) = \frac{Z_1}{(Z_1 - Z_E)}i_L(s) \tag{16}$$

And, substituting (8a) and (8b) in (15),

$$i_E(s) = \frac{sC_1 r_1 + 1}{(sC_1(r_E - r_1) + 1)} i_L(s) \tag{17}$$

This is the relation between inductor current and input source current. Now, a relation of input current as the function of output ripple current and duty variation is obtained as given by (18). This is done by expanding the equation (17) using (10) in it, and rearranging the coefficients of numerator and denominator of polynomials in terms of the input capacitance, output capacitance and inductance. The constants in (18) are, $A_{11} = r_1 A_1, A_{12} = r_1 A_2, A_{13} = \mu\alpha, A_{14} = r_1 A_3, A_{15} = \mu A_6, A_{16} = r_1 A_5, A_{17} = \mu D'_o, A_{18} = I_L A_{17}, A_{19} = \delta\gamma, A_{20} = \delta A_9, A_{21} = \gamma + \delta, A_{22} = (A_9 + \delta A_{10}), A_{23} = \gamma\delta {D'_o}^2, A_{24} = {A_0}^2 A_{21}$

V. ANALYSIS OF SHC

For the analysis of SHC ripple in frequency domain, a transfer function, output ripple current to input source ripple current ($G_{i_E vs i_o}(s)$), is obtained for $d(s) = 0$. This transfer function is nothing but back current gain of boost converter, given by (19).

$$i_E(s) = \frac{C_1^2 C_2 (A_{11} i_o(s) + A_{12} d(s)) s^3 + [(A_{13} C_1 C_2 + A_{14} C_1^2) i_o(s) + (A_{15} C_1 C_2 + A_{16} C_1^2) d(s)] s^2 + [(A_{17} C_1 + A_4 C_2) i_o(s) + (A_{18} C_1 + A_6 C_2) d(s)] s + A_7 d(s) + A_0 i_o(s)}{A_{19} C_1^2 C_2 L s^4 + C_1 C_2 (A_{20} C_1 + A_{21} L) s^3 + (A_{22} C_1 C_2 + L C_2 + A_{23} C_1^2) s^2 + (A_{24} C_1 + A_{10} C_2) s + {A_0}^2} \tag{18}$$

$$G_{iEvsio}|_{d(s)=0} = \frac{i_E(s)}{i_o(s)} = \frac{A_{11} C_1^2 C_2 s^3 + (A_{13} C_1 C_2 + A_{14} C_1^2) s^2 + (A_{17} C_1 + A_4 C_2) s + A_0}{A_{19} C_1^2 C_2 L s^4 + C_1 C_2 (A_{20} C_1 + A_{21} L) s^3 + (A_{22} C_1 C_2 + L C_2 + A_{23} C_1^2) s^2 + (A_{24} C_1 + A_{10} C_2) s + {A_0}^2} \tag{19}$$

Increase/decrease in the magnitude of back current gain causes increases/decreases the SHC ripple factor in input source. So, the back current gain is an important factor for SHC analysis. The back current gain do not depend on duty variation, so the effect of the size of boost converter's storage elements, on the SHC ripple in input source is analyzed in this section. This is why, the transfer function is expressed as the function of L, C_1 and C_2. Further simplification of $G_{iEvsio}(s)$ by neglecting ESRs (except ESR of inductor) in (19) gives,

$$G_{iEvsio}(s)|_{d(s)=0} = \frac{\frac{D'_o}{LC_2}}{s^2 + \frac{r_L}{L}s + (\frac{D'_o}{\sqrt{LC_2}})^2} \tag{20}$$

$$Damping\ ratio, \zeta = \frac{r_L}{2D'_o}\sqrt{\frac{C_2}{L}} \tag{21a}$$

$$Natural\ frequency, \omega_n = \frac{D'_o}{\sqrt{LC_2}} \tag{21b}$$

Now substituting $s = j\omega$ in (24), we have

$$G_{iEvsio}(s)(j\omega)|_{d(j\omega)=0} = \frac{1 - \frac{\omega^2}{{\omega_n}^2} - j2\zeta\frac{\omega}{\omega_n}}{D'_o[1 + \frac{\omega^4}{{\omega_n}^4} - (2 - 4\zeta^2)(\frac{\omega^2}{{\omega_n}^2})]} \tag{22}$$

The magnitude of back current gain is,

$$|G_{iEvsio}(j\omega)|_{d(j\omega)=0}| = \frac{1}{D'_o\sqrt{1 + \frac{\omega^4}{{\omega_n}^4} - (2 - 4\zeta^2)(\frac{\omega^2}{{\omega_n}^2})}} \tag{23}$$

And, phase of the back current gain is,

$$\angle G_{iEvsio}(j\omega)|_{d(j\omega)=0} = -tan^{-1}(\frac{2\zeta\omega_n\omega}{{\omega_n}^2 - \omega^2}) \tag{24}$$

Lets $\omega_2 = 2\omega$ is second order ripple frequency. This is the frequency, in which, we are interested. In our case, inverter output frequency is 50 Hz. This is why ω_2=100Hz. Using (23) and (24), magnitude and phase angle of the back current gain at ω_2 for different value of natural frequency, (ω_n) can be deduced as follows,

$$|G_{iEvsio}(j\omega_2)|_{d(j\omega_2)=0}| \approx \begin{cases} \frac{1}{D'_o} & \omega_n \gg \omega_2 \\ \frac{1}{2\zeta D'_o} & \omega_n = \omega_2 \\ 0, & \omega_n \ll \omega_2 \end{cases} \tag{25a}$$

$$\angle G_{iEvsio}(j\omega_2)|_{d(j\omega_2)=0} \approx \begin{cases} -180 & \omega_n \gg \omega_2 \\ -90 & \omega_n = \omega_2 \\ 0 & \omega_n \ll \omega_2 \end{cases} \tag{25b}$$

The effect of the size of inductor, input capacitor and output capacitor of boost converter, on the back current gain, and hence on SHC ripple, is discussed henceforth.

A. *Effect of the Size of the Inductor* (L)

The variables in equation (23) are ω_n and ζ only. In (21a), ζ is proportional to r_L and inversely proportional to $\sqrt{L}$ for the fixed size of C_2. The r_L of inductor increases with the increase in size of L. This increases ζ. ω_n is inversely proportional to $\sqrt{L}$. To observe the effect of the size of L, on the back current gain, we keep the C_1 and C_2 fixed. For small size of L, the natural frequency and damping ratio are large, this implies $\omega_n \gg \omega_2$. Using this in (23) gives almost constant value of back current gain at ω_2 in low frequency range which is given by (25a). Increase in L decreases ω_n and ζ, this results in increase in resonance peak toward the lower frequency. This may be possible that, for a given value of L, $\omega_n = \omega_2$. For this condition, gain can be given by (25a). At this frequency ζ is small and hence back current gain is high. This leads to a large SHC ripple in input source. This condition must be avoided. The inductor size must be chosen carefully. Further increase in L, reduces ω_n. For a very large value of L, $\omega_n \ll \omega_2$. This condition results in a very less back current gain at ω_2, but some frequencies lower than ω_2 may overshoot. This can be seen in bode plot shown in Fig:5a also. The figure shows bode plots of G_{iEvsio} for five different values of L, keeping C_1 and C_2 fixed.

B. *Effect of the size of output capacitor* (C_2)

The effect of the size of output side capacitor of boost converter, on the back current gain and hence on SHC ripple in input source, is discussed in this section. To analyze the effect of the size of C_2 on the back current gain, the L and C_1 are kept fixed. ζ increases with increase in C_2, while ω_n decreases. For the small size of C_2, ω_n and resonance peak are large, this can be deduced from (21). For $\omega_n \gg \omega_2$, the magnitude of back current gain is constant at ω_2, as given by (25a). Increasing the size of capacitor, ω_n and resonance peak decreases towards lower frequencies. For $\omega_2 = \omega_n$, the back current gain is very less. This is because of large value of ζ. This reduces back current gain ($\frac{1}{2\zeta D'_o}$) as given by (25a). Further increase in C_2, significantly reduces back current gain. This concludes that, increasing the size of output side capacitor, the high and low both frequency can be reduced in input source. This is also shown in Fig:5b, using bode plot. The plot is shown for five different value of C_2, keeping L and C_1 fixed. A large size of output side capacitor is an effective solution but not efficient one.

C. *Effect of the size of input capacitor* (C_1)

Clearly, (20) do not have C_1 term. This implies that the effect of C_1 is negligible on back current gain. The same conclusion can be drawn using Bode plot. Fig:5c, shows bode plots for five different values of input capacitance, with L and C_2 fixed. There is negligible change in back current gain in low frequency region along with 100 Hz.

VI. System Validation

In this section, validation of proposed theoretical circuit with experimental has been done. A prototype of boost converter feeding inverter load is shown in Fig:4. Real time digital simulator (RTDS) is chosen as the control platform. Experimental results are obtained using system parameters from the Table-I. Similarly, equivalent circuit has been simulated on MATLAB-Simulink using the same parameters and results are taken at various measurement points of boost converter. Simulation and experimental results are taken for

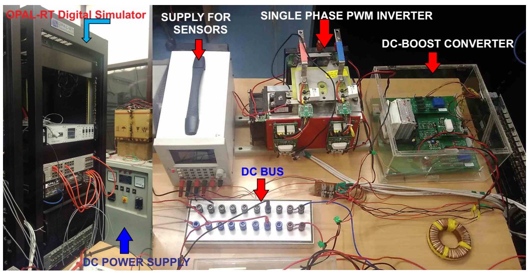

Fig. 4. Experimental setup

(a) output voltage (b) output current (c) inductor current (d) input source current. Simulation and hardware results are shown in Fig.6. In each figure, top part is experimental result (ER1,ER2,ER3,ER4) and bottom part is simulation result (SR1,SR2,SR3,SR4). Each simulation result also shows the

TABLE I
System Parameters

Parameter	Value
Boost converter	
(a) Input voltage, (E) and ESR	$50V$ and 0.01Ω
(b) Output voltage, V_o	$100V$
(c) DC bus resistive load and power	1200Ω, $8.4W$
(d) Inductance (L) ,ESR (r_L)	$2.1\ mH$, $225m\Omega$
(e) Input capacitor (C_1), ESR (r_1)	$22\mu F$, 2.5Ω
(f) Output capacitor (C_2), ESR (r_2)	$22\mu F$, 2.5Ω
(g) DC bus resistive load	1200Ω
(h) Duty cycle, D_o	50%
(i) IGBT on state resistance (r_S)	$93.3m\Omega$
(j) Diode on state resistance (r_D)	$113m\Omega$
(k) Diode on state voltage drop (V_D)	$1.7V$
(l) Switching frequency	$25000kHz$
Single phase PWM inverter	
(a) Load resistance and power	205Ω, $32W$
(b) Switching frequency	$5000kHz$

magnitude of $100Hz$ frequency component in overall signal and total harmonic distortion (THD). Note: Scaling factor of simulation and experimental voltage results is 0.005 (i.e. actual signal multiplication factor=200). Scaling factor of current measurement is 1. For magnitude comparison of these waveform, a Table-II is also shown. First column of Table-II contains the current and voltage on different measurement points of boost converter. These measurements contain mean value, peak to peak value (P-P) of ripple, and percentage of P-P ripple with respect to mean value, $(\%Ripple)$. In second and third columns, experimental results (ER) and simulation results (SR) are tabulated respectively. Forth column contains the error between ER and SR i.e. E_r. Shapes and magnitudes of simulation and experimental results are nearly congruent. Furthermore, it can also be concluded that the input capacitor negligibly check the propagation of SHC in source. This can be observed by comparing results of the Fig.6c and Fig:6d. Both waveforms are similar which is possible only, if the inductor ripple current passes directly to the input source without being bypassed by input side capacitor.

TABLE II
COMPARISON

Measurement	**ER**	**SR**	$\mathbf{E_r}$
Output voltage			
$Mean$	97.4V	96V	1.4V
$Peak\ to\ Peak$	5.57V	7V	-1.43V
$\%\ Ripple$	5.68%	7.1%	
Output current			
$Mean$	0.25A	0.31A	0.06A
$Peak\ to\ Peak$	0.3857A	0.36A	0.0257A
$\%\ Ripple$	154%	116%	
Inductor current			
$Mean$	0.443A	0.614A	-0.171A
$Peak\ to\ Peak$	0.6788A	0.67A	0.088A
$\%\ Ripple$	153%	109%	
Input current			
$Mean$	0.5A	0.6225A	-0.1225A
$Peak\ to\ Peak$	0.79A	0.68A	
$\%\ Ripple$	158%	109%	

VII. Conclusion

The proposed equivalent circuit captures the dynamics of ripple. The study and analysis concludes that the output capacitor has a substantial impact in ripple reduction. A large size inductor can reduce the SHC ripple in input source but at the same time, it may introduce low frequency noise. Input capacitor of boost converter shows negligible effect on ripple. This shows congruence between simulation and experimental results.

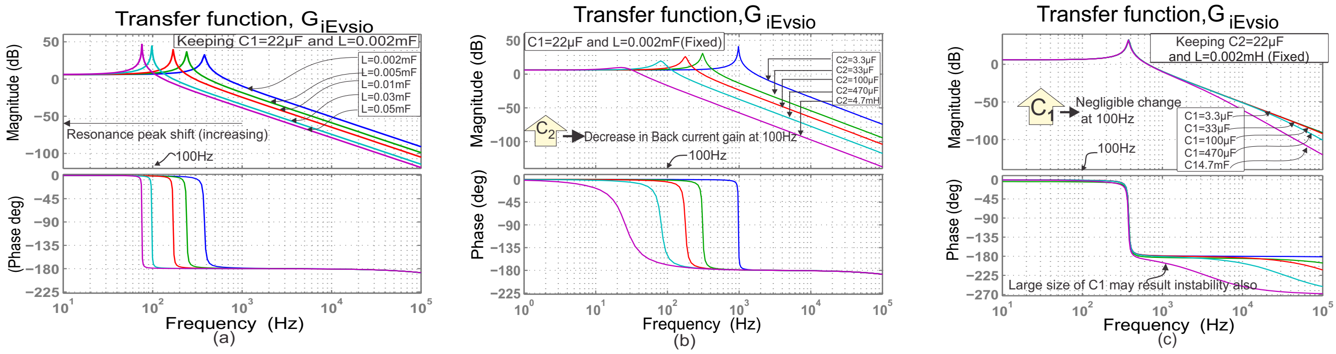

Fig. 5. Bode plot of G_{iEvsio}:effect of variation in (a) L, (b) C_2, and (c) C_1

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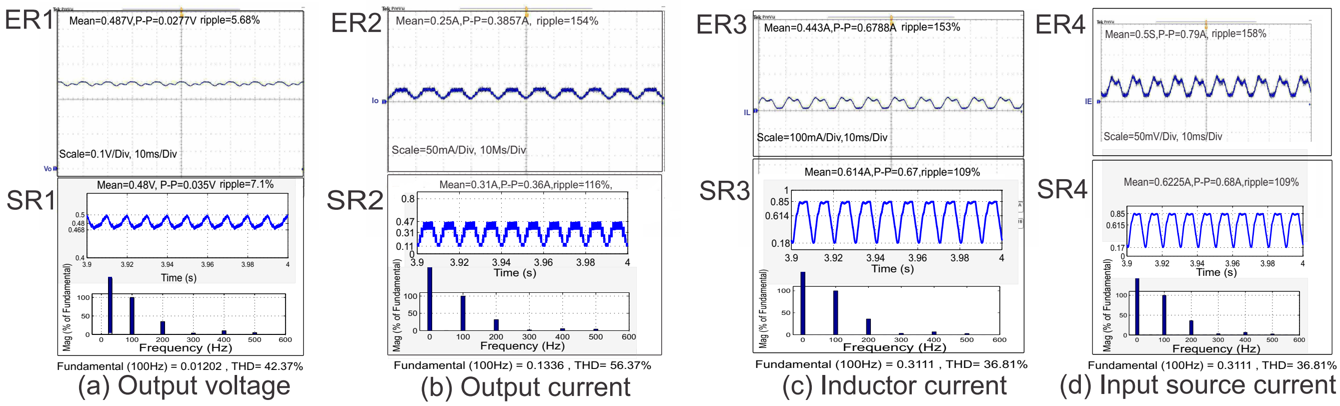

Fig. 6. Comparison of simulation and experimental results

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